ABSTRACT

To speed up the operation of a decoder circuit, reduce the power consumption of the decoder circuit and increase the cycle, each circuit such as a buffer, a predecoder and a main decoder in the decoder circuit is composed by a semiconductor logic circuit wherein the number of columns of transistors for pulling down at an output node is small even if the number of inputs is many and the true and a complementary output signal having approximately the same delay time are acquired and the output pulse length of each circuit in the decoder circuit is reduced.

According to the present invention, the operation of the decoder circuit can be sped up, the power consumption can be reduced, the cycles can be increased and in a semiconductor memory for example, the reduction of access time and power consumption and the increase of the cycles are enabled.